Lecture-1

1. **What is Moore’s Law? Why and how was it modified in 1975?**

Page 16. Page 18.

1. **What is the impact of Moore’s law on the development of VLSI?**
2. **Explain the brief history of IC industry.**

Page 12-14.

1. **Explain the different steps in VLSI realization process.**

Page 23.

1. **What are the problems of VLSI design on today?**

Page 24.

1. **How do you define LSI and VLSI?**

Page 26.

1. **What is yield? How cost is related to yield in chip designing?**

Page 28-29.

1. **What is verification?**

Page 31.

1. **Explain VLSI design Cycle.**

Page 32.

**Lecture-2**

1. **What is semiconductor?**

Page 2.

1. **Explain the Energy Band theory of crystal.**

Page 8-13.

1. **In the light of energy band theory, explain semiconductor, metal, insulator.**

Page 13.

1. **Why Si, Ge are semiconductors?**

Page 14-17.

1. **What are holes? Explain how holes can be carrier of electricity.**
2. **What is doping in semiconductor? What are its effects?**

Page 18.

1. **Explain donor and acceptor impurity in semiconductors?**

Page 16-17.

1. **What is semiconductor diode? What is depletion region? Explain the operation of semiconductor diode with both forward and reverse biased.**

Page 19-23.

1. **Explain Bipolar junction transistor.**
2. **Explain its three modes of operation of a bipolar transistor.**

Page 30-31.

1. **How does bipolar transistor act as an amplifier?**

Page 35-36.

1. **How does transistor act as a switch?**

Page 40.

1. **Compare the operations of semiconductor diode and transistor.**

**Lecture-3**

1. **What are the problems of bipolar junction transistor?**

Page 2.

1. **Classify Field effect transistors.**

Lect-4 page 20.

1. **Sketch the basic structure of an n-channel field effect transistor.**

Page 4.

1. **Explain the characteristics of JFET. How does it behave for small VDS and large VDS? How and when it turns from ohmic region to saturation region?**

Page 6-7.

1. **Define pinch-off voltage. Sketch the depletion region before and after pinch-off.**
2. **Explain JFET as amplifier and switch.**
3. **Compare bipolar junction transistor versus junction field effect transistor.**

<http://www.learningaboutelectronics.com/Articles/BJT-vs-FET.php>

**Lecture-4**

1. **Explain MOSFET. What are the advantages of MOSFET over JFET?**

Page 2-8.

1. **Explain MOSFET with both enhancement and depletion mode.**
2. **Explain how MOSFET act as a switch.**
3. **Compare p channel and n channel MOSFET**
4. **Classify different Field Effect transistors.**

Page 20.

1. **Compare the transfer characteristics in JFET, depletion type MOSFET, enhancement type MOSFET.**
2. **Compare Silicon versus Germanium in the use of chip designing.**

Lect 8.

1. **Explain the functioning of nMOS inverter considering the load as a) resistor b) enhancement type transistor c) depletion type transistor.**
2. **What is the problem of the nMOS inverter with pull up as an enhancement type? How is it improved with depletion type pull up?**
3. **What are the drawbacks of MOSFETs?**

Page 34.

1. **What are the advantages of CMOS over MOSFET? What are the disadvantages of CMOS design?**
2. **How does CMOS work as an inverter?**

Page 40.

**Lecture-5**

1. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of nMOS.**
2. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of pMOS.**
3. **Implement the Boolean function *f=* *ab*+ + *abd+*+ *acd* with the help of a) CMOS Nand CMOS Nor.**
4. **What is single complex cell design in CMOS? What are its advantages and disadvantages of it?**
5. **Implement the Boolean function *f=* *ab+*+ *abd +*+ *acd* using single complex cell designs in four different ways (consider that for any input, its complement is also available).**
6. **How are the circuits optimized at different levels?**

Page 19.

**Lecture-6**

1. **What is the significance of stick diagram, as applicable in the design of VLSI?  What is its advantage and limitation?**

Page 27-30.

1. **Draw the layout of NAND and NOR using CMOS designs.**
2. **How to reach mask diagram from stick diagram.**
3. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions :**

**i)                     f =  A`B  + Ā`C [ using n MOS transistors]**

**ii)                   g = ( w +x + z). (`w  + xz )  [ using C MOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = W `XZ + `W`Y  [ using n MOS transistors]**

**(ii) g = (A + `B + D) (`A + BD) [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = A`B + `AC +`CD  [ using n MOS transistors]**

**(ii) g = (w + `x ) (`y + z) [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = (w+`x +`z) (`w+y+x)  [ using n MOS transistors]**

**(ii) g =  `AC`D + A`BC [using CMOS transistors ]**

1. **Draw the coloured stick and mask diagrams for implementing the following Boolean functions : (i) f = A`BC + `AB`C  [ using n MOS transistors]**

**(ii) g = (`w +x+z) (w+`x +`z) [using CMOS transistors ]**

1. **Draw the stick diagram of a shift register cell using a transmission gate followed by a CMOS inverter.**
2. **Convert the stick diagram obtained in previous question to symbolic form and show an example of optimization in it.**

**Lecture-7**

1. **Discuss the problems of manufacturing in sizing of the different elements in fabrication.**

Page 5-6.

1. **What is design rule? What is the advantage of generalized design rule?**

Page 2,8.

1. **What do you mean by l–based IC design rules?**

Page 9.

1. **What are the rules of design rules?**

Page 14-16.

1. **Explain nMOS design rules.**

Page 20-27.

1. **Explain buring contact and butting contact in nMOS design. Compare their merits and demerits.**
2. **Explain CMOS design rules.**
3. **Explain the design rules for different contact cuts.**
4. **Explain the design rules for via and cut.**
5. **For a CMOS shift register cell (as in question 56 and 57) draw the mask diagram conforming the l–based design rules.**

**Lecture-8**

1. **Compare silicon versus Germanium in fabrication.**

Page 2.

1. **Why is silicon preferred for fabrication?**

Page 2.

1. **How the silicon wafer is prepared from sand? Explain the steps.**

Page 5-8.

1. **What is photoresist? Explain its uses in fabrication process.**

Page 11. Page 14.

1. **Define lithography.**

Page 9.

1. **Explain the basic processing steps in fabrication.**

Page 10.

1. **Describe etching process.**

Page 14.

1. **What is the role of silicon dioxide in fabrication?**
2. **Explain the different steps in nMOS fabrication.**

Page 19.

1. **What is polysilicon? What is its use in fabrication process?**

Page 20-21.

1. **Explain the chemical vapour deposition technique.**

Page 24-25.

1. **Explain the different fabrication steps in CMOS. Compare the p-well and n-well process in CMOS fabrication.**

Page 27-43. Page 44.

**Lecture-9**

1. **What is partitioning? Why do we need it?**

Page 9.

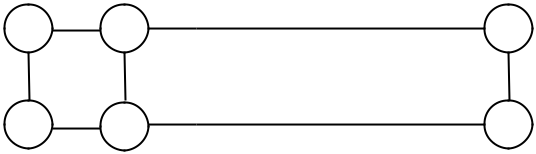
1. **What are the different levels of partitioning?**

Page 11.

1. **Consider a hypergraph H, where each hyperedge interconnects at most three vertices. We model each hyperedge of degree-3 with three edges of weight ½, on the same set of vertices, to obtain a weighted graph G. Prove that an optimal balanced partitioning of G corresponds to an optimal balanced partitioning of H.**
2. **In refer to Question 3, prove that optimal balanced partitioning of G cannot be done if each edge of H interconnects at most four vertices (i.e., give a counter example).**
3. **Explain Kernighan-Lin algorithm for partitioning a graph. Find its time complexity.**

Page 21-25.

1. **Consider a path graph v1, v2,….., vn. That is, v1 is connected to vi+1, for 1 < i < n-1. Apply the Kernighan-Lin algorithm to this graph. As the initial partition, let va, for all odd values of a be in one set , and vb, for all even values of b, be in the other set.**
2. **Consider a complete binary tree with n nodes. Apply Kernighan-Lin algorithm to this graph. As the initial partition, let va, for all internal vertices, be in one set and vb, for all leaves, be in the other set.**
3. **Show how the Kernighan-Lin Heuristic works on the ladder graph with 2n vertices, starting with initial partition of V1= {1,2,3,……,n}, and V2={n+1,n+2,n+3,…..,2n}.**

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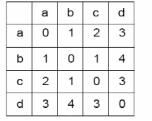
|  |  |  |
| --- | --- | --- |
| **1** | **2** | **n** |
| **n+1** | **n+2** | **2n** |

**Fig. 1**

1. **What are the drawbacks of Kernighan-Lin algorithm?**

Page 26.

1. **The following matrix provides 4 modules a,b,c,d with their entries representing the number of connections between the two modules. Apply Kernighan-Lin heuristic to obtain the partitioning.**

****

**Fig.2**

**Lecture-10**

1. **What are the advantages of Fiduccia-Mattheyses algorithm over Kernighan-Lin algorithm?**

Page 2.

1. **What are the similarities between Fiduccia-Mattheyses algorithm and Kernighan-Lin algorithm?**
2. **Present the Fiduccia-Mattheyses Algorithm. Find out its time complexity.**

Page 8. Page 12.

1. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 7.**
2. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 8.**
3. **Apply Fiduccia-Mattheyses Algorithm for the problem in question 10.**
4. **“There is a trade off associated for partitioning with replication.” Is it true or false? Justify.**
5. **Discuss how Partitioning is affecting overall delay.**
6. **What do you understand by performance driven partitioning?**

Page 20.

1. **Discuss the approach of clustering in case of partitioning.**

Page 23.

**Lect 11-12**

1. **Define Floor planning. Define sliceable and non-sliceable floorplan with examples. What are the advantages of sliceable floorplan?**

Lect 11 Page 3-4. Page 6,8. Page 7.

1. **State with an example how a sliceable floorplan can be represented by a binary tree.**

Lect 11 Page 10.

1. **When an adjacency graph cannot admit a rectangular dual?**

Page 20.

**14. Obtain the hierarchical floorplan tree for the floorplan given in Fig.5.**

**15. Illustrate the steps of rectangular dualization on an inherently non-sliceable graph of n vertices.**

**16. Obtain a rectangular dual of the following adjacency graph.**

**Fig. 3**

**17. Obtain the rectangular dual of the following adjacency graph below of Fig. 4.**

**18. Are the Floorplans obtained in 17 and 18 sliceable?**

**19. Prove that there is a one-to-one correspondence between a sliceable floorplan and a normalized Polish expression.**

**20. Give the adjacency graph for the following floorplan of Fig.5.**